B11

(12) UK Patent Application (19) GB (11) 2 342 777 (13) A

(43) Date of A Publication 19.04.2000

(21) Application No 9924488.1

(22) Date of Filing 15.10.1999

(30) Priority Data
(31) 10294905 (32) 16.10.1998 (33) JP

(51) INT CL[7]
H01L 27/088 21/8234

(52) UK CL (Edition R)
H1K KGAGX K1CA K11B4 K11D K11D1 K4C14 K9C2 K9D1

(56) Documents Cited
GB 2001197 A US 5495122 A US 4651406 A

(58) Field of Search
UK CL (Edition R) H1K KCAL KGAGX
INT CL[7] H01L
ON LINE,W.P.I.,EPODOC,JAPIO

(71) Applicant(s)
NEC Corporation
(Incorporated in Japan)
7-1 Shiba 5-chome, Minato-ku, Tokyo 108-01, Japan

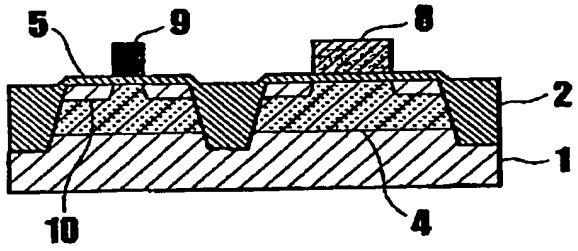
(72) Inventor(s)
Kiyotaka Imai

(74) Agent and/or Address for Service
Mathys & Squire
100 Grays Inn Road, LONDON, WC1X 8AL,
United Kingdom

(54) Abstract Title
Gate electrodes for integrated mosfets

(57) A plurality of MOSFETs of one conductivity type having gate electrodes 8,9 formed of a semiconductor material are formed in a semiconductor substrate 1. The gate electrodes of these MOSFETs are implanted with an impurity at different concentrations in accordance with the threshold voltages to be set for the MOSFETS. Initially, an isolation region 2 and wells 4 are formed on the surface of the semiconductor substrate. Then a gate oxide film 5 is formed on the surfaces of the isolation region and the well. A polysilicon film for forming gate electrodes is then grown on the surfaces of the gate oxide film and the isolation region. A resist is then deposited to allow ion implantation in one gate region of the polysilicon film but prevent implantation in the other gate region After removing the resist and patterning the polysilicon film to form first and second gate electrodes 8,9 a second impurity is implanted in the first and second gate electrodes and prospective source/drain regions 10.

FIG. 3F



GB 2 342 777 A

FIG. 1 PRIOR ART

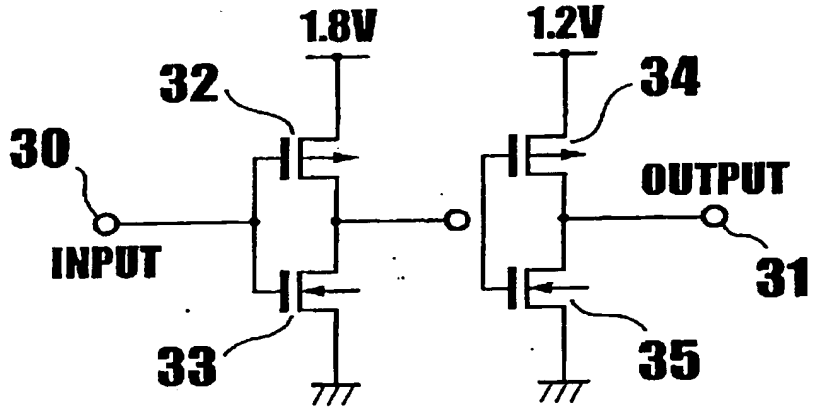


FIG. 2A PRIOR ART

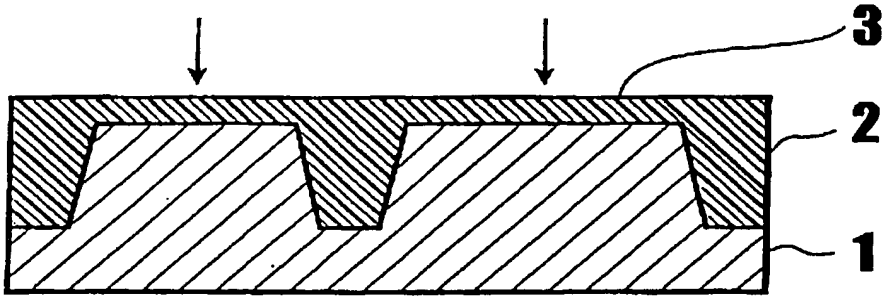


FIG. 2B PRIOR ART

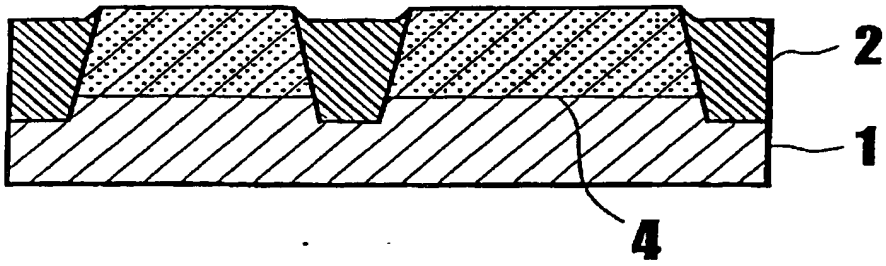


FIG. 2C PRIOR ART

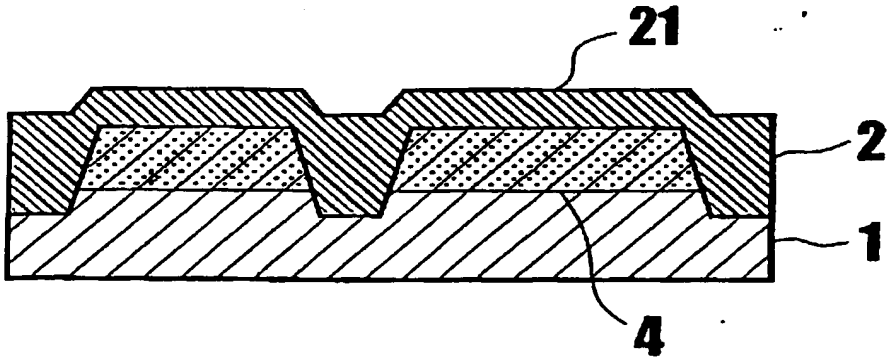


FIG. 2D PRIOR ART

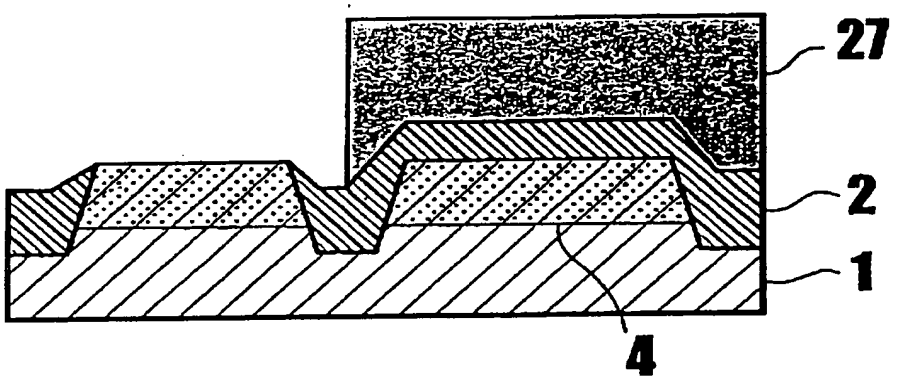


FIG. 2E PRIOR ART

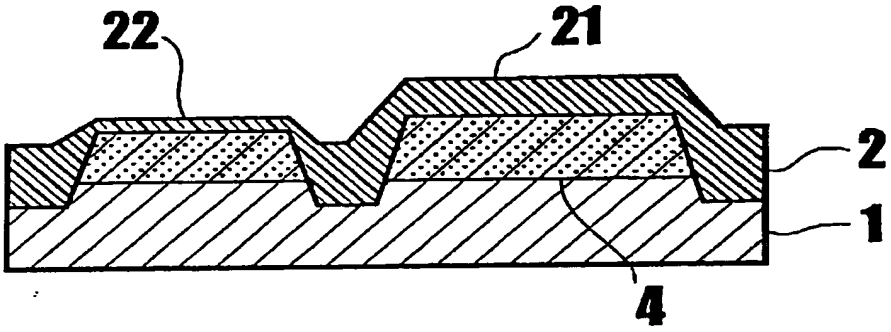


FIG. 2F PRIOR ART

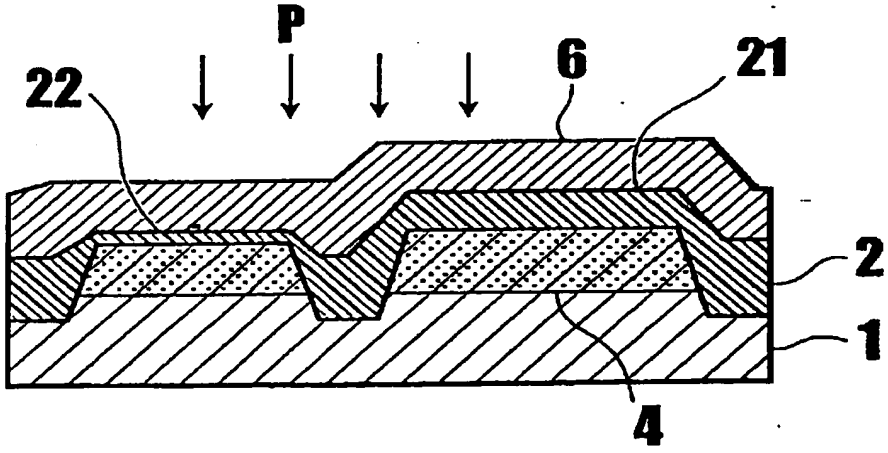


FIG. 2G PRIOR ART

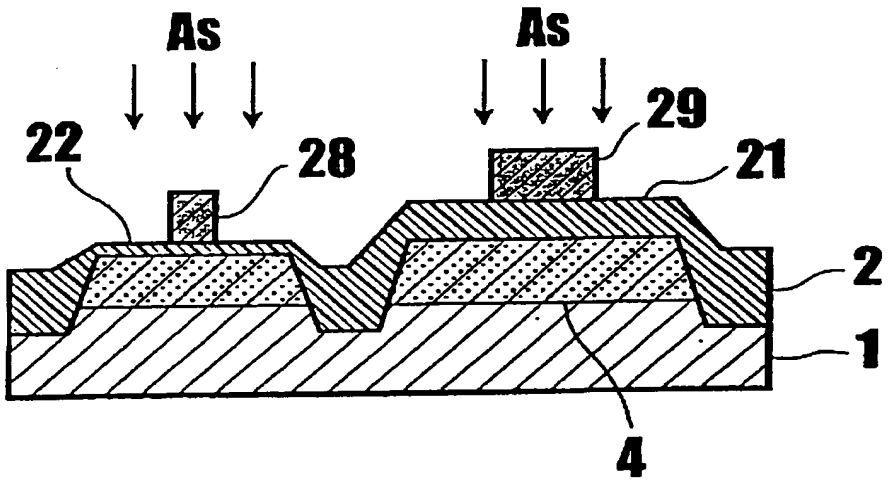


FIG. 2H PRIOR ART

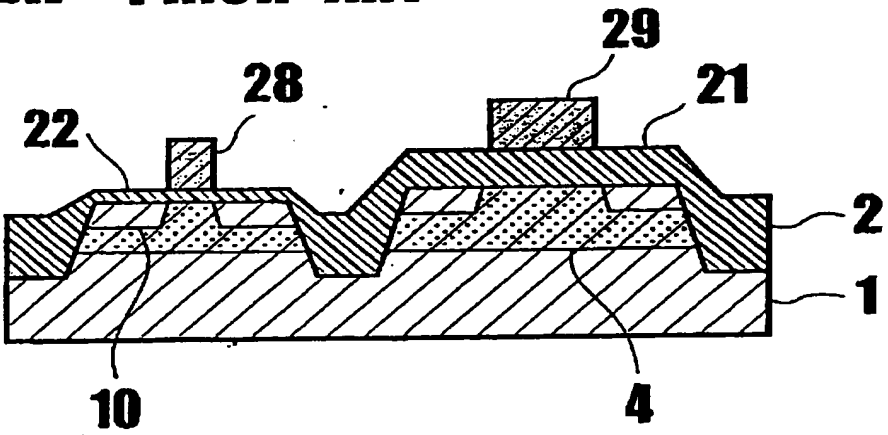


FIG. 3A

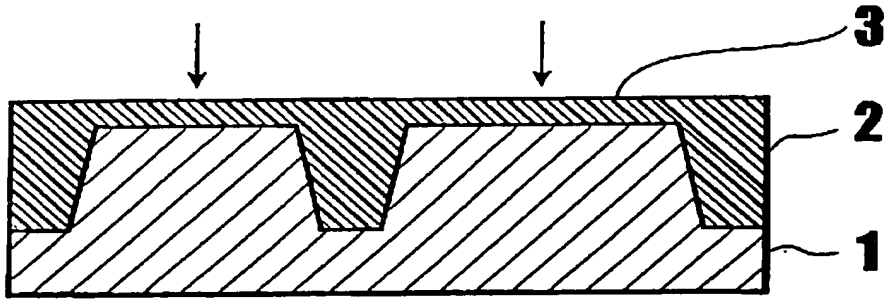


FIG. 3B

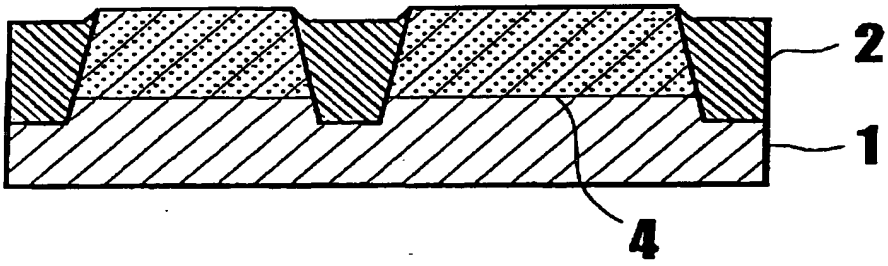


FIG. 3C

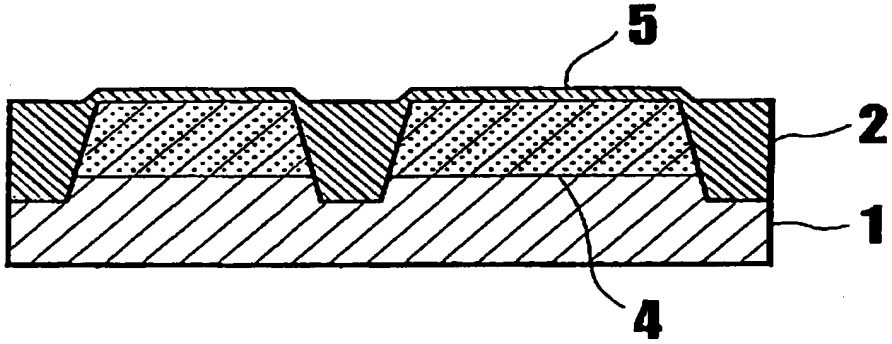


FIG. 3D

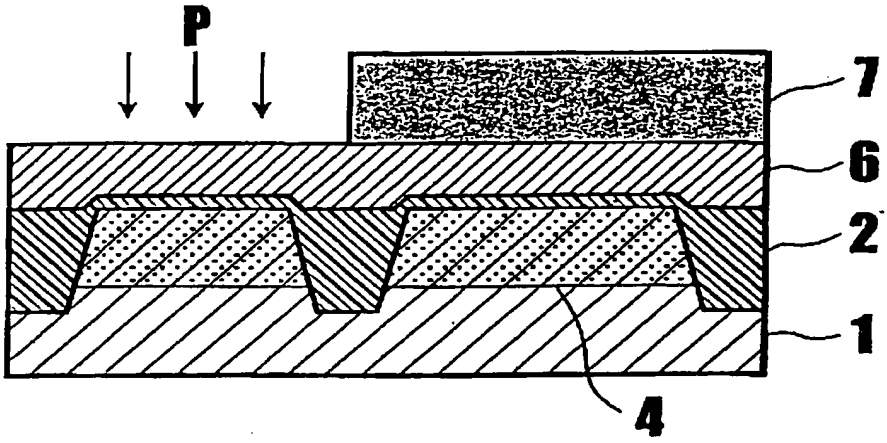


FIG. 3E

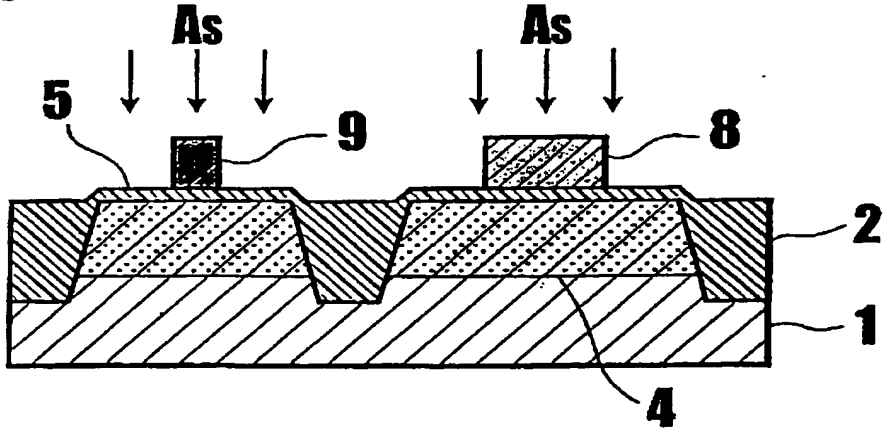


FIG. 3F

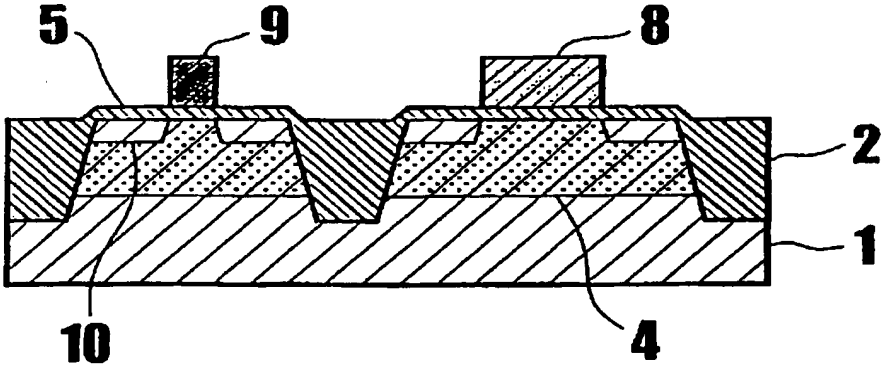


FIG. 4

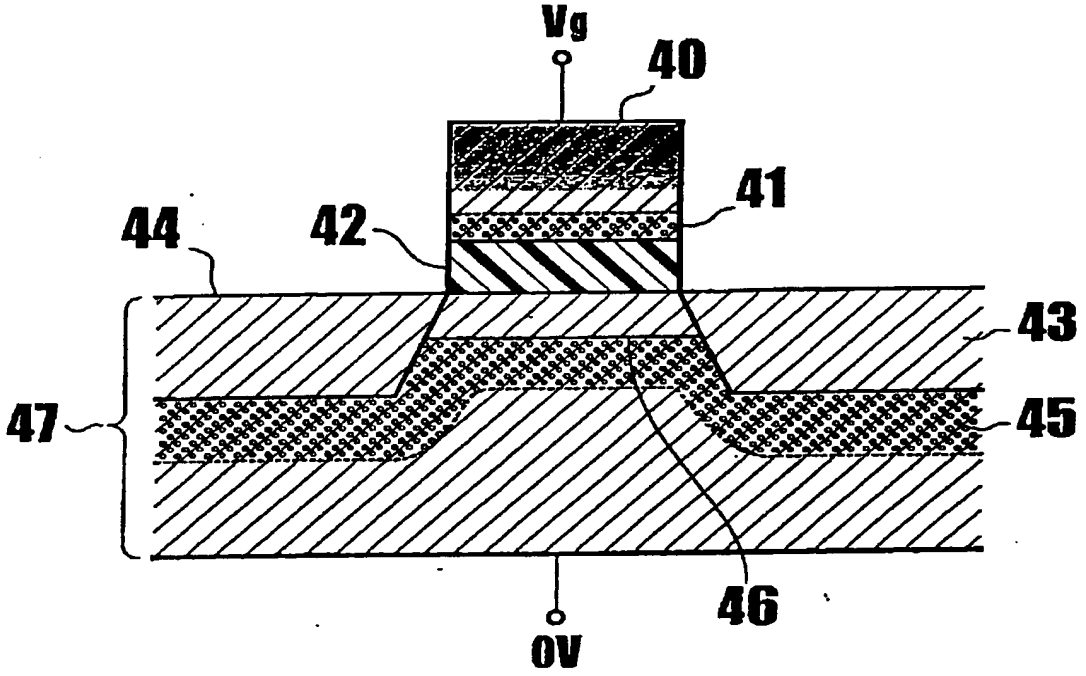
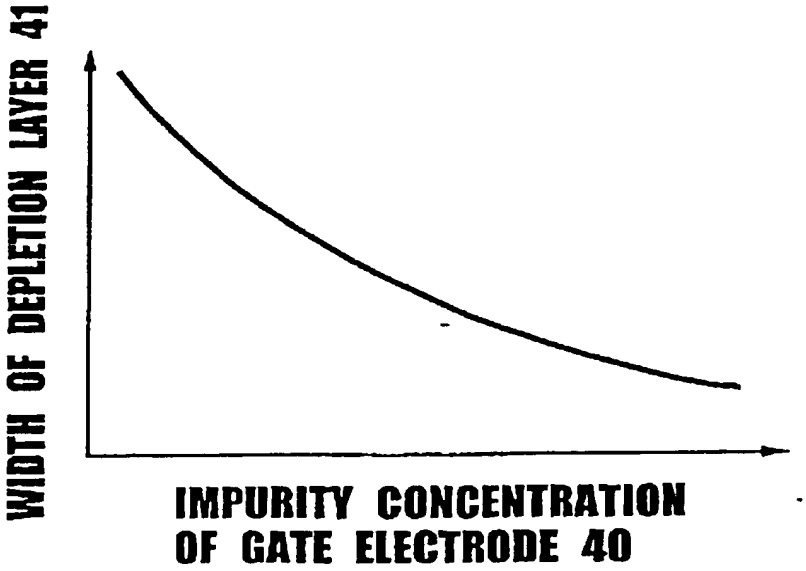

Vg
40
41
42
44
43
47
45
46
0V

FIG. 5


WIDTH OF DEPLETION LAYER 41
IMPURITY CONCENTRATION
OF GATE ELECTRODE 40

SEMICONDUCTOR DEVICE HAVING A PLURALITY OF MOSFETS ON SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a semiconductor device and a method of manufacturing the same and, more particularly, to a semiconductor device in which a plurality of MOSFETs having different threshold voltages are formed on one semiconductor substrate, and a method of manufacturing the same.

Description of the Prior Art:

Generally, in a MOSFET, when the thickness of the gate oxide film is decreased to reduce the threshold voltage, although the operation speed rises, the OFF current and the gate direct tunnel current increase. When the thickness of the gate oxide film is increased to raise the threshold voltage, although the operation speed drops, the OFF current and the gate direct tunnel current decrease. A gate direct tunnel current is a current that flows from a gate electrode to a channel through a gate oxide film when a voltage is applied to the gate electrode.

In designing a MOSFET constituting the circuit of a semiconductor device, a MOSFET having an optimum-thick

gate oxide film must be used considering the specification, characteristics, and the like required for the semiconductor device. For this purpose, a plurality of types of MOSFETs having different gate oxide film thicknesses must be formed on one semiconductor substrate.

When the power supply voltage is decreased to lower the power consumption and the like, a plurality of circuits that operate on different power supply voltages are sometimes formed on one semiconductor substrate. In this semiconductor device, the threshold voltages of the MOSFETs forming the respective circuits must be set at values suitable for the power supply voltages to be applied. Therefore, a plurality of MOSFETs having different gate oxide film thicknesses must be formed on one semiconductor device.

For example, a circuit unit shown in Fig. 1 is obtained by mounting a circuit having a power supply voltage of 1.8 V and a circuit having a power supply voltage of 1.2 V so as to be adjacent to each other. In this circuit unit, an inverter comprised of a p-channel MOSFET 32 and an n-channel MOSFET 33, and an inverter comprised of a p-channel MOSFET 34 and an n-channel MOSFET 35 are so mounted on a semiconductor substrate as to be adjacent to each other. The source electrode of the p-channel MOSFET 32 is connected to the 1.8-V power supply

voltage, and that of the p-channel MOSFET 34 is connected to the 1.2-V power supply voltage.

To operate the MOSFETs constituting the circuits driven by different power supply voltages in this manner in an optimum manner, the threshold voltages must be set at different values. To set different threshold voltages, the thicknesses and gate lengths of the gate oxide films of the respective MOSFETs must be set different considering the hot carrier lifetimes of the MOSFETs.

For example, in MOSFETs on one semiconductor substrate, their gate oxide film thicknesses and gate lengths must be set at different values, e.g., the thickness and gate length of the gate oxide film of the n-channel MOSFET 33 that operate on the 1.8-V power supply voltage are respectively set to 35 Å and 0.18 μm, and those of the gate oxide film of the n-channel MOSFET 35 that operate on the 1.2-V power supply voltage are respectively set to 25 Å and 0.13 μm. To set different gate lengths for different MOSFETs on one semiconductor substrate is not particularly difficult, because only the patterning size of the gates need be set different. When compared to this, to set different gate thicknesses for different gate oxide films is not easy.

In a conventional semiconductor device manufacturing method, a multi-oxide process is used to form two types of

MOSFETs having different gate oxide film thicknesses on one semiconductor substrate.

The conventional semiconductor device manufacturing method using this multi-oxide process will be described with reference to Figs. 2A to 2H.

As shown in Fig. 2A, an isolation region 2 and a 100-Å thick sacrificial oxide film 3 are formed on the surface of a p-type silicon substrate 1. P-well implantation and gate boron implantation are performed through the sacrificial oxide film 3.

As shown in Fig. 2B, the sacrificial oxide film 3 is removed by etching. To completely remove the sacrificial oxide film 3 by etching, overetching is performed to remove the surface of the structure for a depth larger than the thickness of the sacrificial oxide film 3. If the overetch amount is 100%, the surface of the isolation region 2 is etched deep from the surface of each p-well 4 by 100 Å.

P-well implantation in the step shown in Fig. 2A forms the p-wells 4 on the surface of the p-type silicon substrate 1.

As shown in Fig. 2C, a 35-Å thick first gate oxide film 21 is formed on the surfaces of the isolation region 2 and p-wells 4.

As shown in Fig. 2D, a resist 27 is formed on the

surface of the first gate oxide film 21 at a region where a MOSFET having a gate oxide film thickness of 35 Å is to be formed, and the first gate oxide film 21 is removed by etching. As a result, the first gate oxide film 21 at a portion where the resist 27 is formed remains to have a thickness of 35 Å. However, during this etching, the surface of the isolation region 2 is removed again by etching.

As shown in Fig. 2E, a 25-Å thick second gate oxide film 22 is formed on a region where a MOSFET having a thin gate oxide film is to be formed. After that, the resist 27 is removed.

As shown in Fig. 2F, a polysilicon film 6 as the material of a gate electrode is grown, and phosphorus (P) is implanted in the polysilicon film 6.

As shown in Fig. 2G, the polysilicon film 6 is patterned and removed by etching, to form gate electrodes 28 and 29. After that, arsenic (As) is implanted in the gate electrodes 28 and 29 and the prospective source/drain regions of their MOSFETs.

Hence, as shown in Fig. 2H, phosphorus and arsenic are implanted in the gate electrodes 28 and 29 as impurities to form source regions (drain regions) 10 in their MOSFETs.

According to this manufacturing method, two types of

MOSFETs having different gate oxide film thicknesses are formed on one p-type silicon substrate 1, as shown in Fig. 2H.

With this multi-oxide process, after the thick gate oxide film is formed, the oxide film on the thin gate oxide film region is removed by etching. After that, oxidation is performed again to form a thin gate oxide film.

For this reason, when removing the oxide film on the thin gate oxide film region by etching, the oxide film on the isolation region is also etched to decrease the oxide film thickness of the isolation region.

The deeper the isolation region, the higher the isolation performance. When, however, the oxide film thickness of the isolation region decreases, a high isolation performance cannot be assured. If the number of types of gate oxide film thickness increases, the manufacture of the semiconductor device sometimes becomes impossible.

To form gate electrodes, a polysilicon film is patterned and removed by etching. If the gate oxide film thicknesses differ, a height difference forms on the surface of the polysilicon film. Then, a focusing error occurs during patterning with an exposing unit, producing an error in gate size such as gate length, gate width, and

the like.

In the conventional semiconductor device described above, when forming MOSFETs having different threshold voltages on one semiconductor substrate, the following problems arise.

(1) Each time a gate oxide film is formed, the isolation region is removed by etching to decrease the thickness of the oxide film of the isolation region.

(2) A focusing error occurs while patterning the gate material to produce an error in gate size.

SUMMARY OF THE INVENTION

An object of the preferred embodiment of the present invention is to address the above problems in the prior art by providing a semiconductor device in which a plurality of MOSFETs having different threshold voltages are formed on one semiconductor substrate without changing the thicknesses of the oxide films of the isolation regions and producing a height difference in the surface of a gate electrode material when patterning the gate electrode material, and a method of manufacturing the same.

According to the first main aspect of the present invention, there is provided a semiconductor device in which a plurality of MOSFETs of one conductivity type having gate electrodes formed out of a semiconductor material are formed

on one semiconductor substrate, and the gate electrodes of the plurality of MOSFETs are implanted with an impurity at different concentrations in accordance with threshold voltages to be set.

The semiconductor device described in the above main aspect has the following subsidiary aspects.

The plurality of MOSFETs of one conductivity type are n-channel MOSFETs.

When the MOSFETs to be formed are n-channel MOSFETs, the impurity to be implanted in the gate electrodes formed of the semiconductor material comprises at least one element selected from the group consisting of arsenic, phosphorus, and antimony.

When the MOSFETs to be formed are p-channel MOSFETs, the impurity to be implanted in the gate electrodes formed of the semiconductor material comprises at least one element selected from the group consisting of boron and indium.

The semiconductor material that forms the gate electrodes comprises silicon.

In order to achieve the above object, according to the second main aspect of the present invention, there is provided a semiconductor device manufacturing method comprising the steps of forming an isolation region and a well on a surface of a semiconductor substrate, forming a

gate oxide film on surfaces of the isolation region and the well, growing a semiconductor material that forms gate electrodes on a surface of the gate oxide film and the surface of the isolation region, forming a film that prohibits ion implantation on that part of a region of the semiconductor material, which forms MOSFETs, in order to set a high threshold voltage therein, implanting a first impurity in the semiconductor material and removing the film that prohibits ion implantation, patterning the semiconductor material and removing the semiconductor material by etching to form first and second gate electrodes, and implanting a second impurity in the first and second gate electrodes and prospective source/drain regions.

According to the present invention, the impurity concentrations of the gate electrodes of the MOSFETs are set different on the basis of threshold voltages to be set. The width of a depletion layer formed on the gate oxide film side of a gate electrode having a high impurity concentration is smaller than that of a gate electrode having a low impurity concentration. The threshold voltage is determined by the sum of the thickness of a gate oxide film and the width of a depletion layer formed in the gate electrode. Accordingly, the threshold voltage of a MOSFET having a gate electrode of a high impurity

concentration is lower than that of a MOSFET having a gate electrode of a low impurity concentration.

Therefore, in the present invention, a plurality of MOSFETs having different threshold voltages can be formed on one semiconductor substrate without decreasing the thickness of the oxide film of the isolation region and producing a height difference in the surface of a gate material when patterning the gate material.

The above and other objects, features and advantages of the present invention should become clear to those skilled in the art upon making reference to the following detailed description and accompanying drawings in which a preferred embodiment incorporating the principle of the present invention is shown by way of illustrative example.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing conventional logical circuits having different power supply voltages;

Figs. 2A to 2H are sectional views sequentially showing steps in manufacturing a conventional semiconductor device;

Figs. 3A to 3F are sectional views sequentially showing steps in manufacturing a semiconductor device according to the present invention;

Fig. 4 is a view explaining a state wherein a voltage

is applied to the gate electrode of a MOSFET; and

Fig. 5 is a graph showing the relationship between the impurity concentration of the gate electrode and the width of the depletion layer in an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will be described with reference to the accompanying drawings.

Figs. 3A to 3F are sectional views showing steps in manufacturing a semiconductor device according to an embodiment of the present invention. In Figs. 3A to 3F, the same reference numerals as in Figs. 2A to 2H denote the same constituent elements.

As shown in Fig. 3A, an isolation region 2 and a 100-Å thick sacrificial oxide film 3 are formed on the surface of a p-type silicon substrate 1. P-well implantation and gate boron implantation are performed through the sacrificial oxide film 3. As shown in Fig. 3B, the sacrificial oxide film 3 is removed by etching. So far the manufacturing steps are identical to those in the conventional semiconductor device manufacturing method.

As shown in Fig. 3C, a 25-Å thick gate oxide film 5 is formed on the surfaces of the isolation region 2 and p-wells 4.

As shown in Fig. 3D, a polysilicon film 6 is grown on the surfaces of the gate oxide film 5 and isolation region 2. After that, a resist 7 is formed on a region where a MOSFET having a high threshold voltage is to be formed. Phosphorus as an impurity of a gate electrode is implanted in the polysilicon film 6. Although the resist 7 is used to prohibit implantation of phosphorus, any film such as a nitride film that can prohibit ion implantation can be used in place of the resist 7.

As shown in Fig. 3E, after the resist 7 is removed, the polysilicon film 6 is patterned and removed by etching to form gate electrodes 8 and 9. Arsenic is implanted in the gate electrodes 8 and 9 and the prospective source/drain regions of their MOSFETs.

As a result, a semiconductor device according to this embodiment is completed, as shown in Fig. 3F. In the MOSFETs of the semiconductor device of this embodiment, only arsenic is implanted in the gate electrode 8, while phosphorus and arsenic are implanted in the gate electrode 9. In other words, in the MOSFETs of the semiconductor device according to this embodiment, although the gate oxide films have the same thickness, the gate electrodes have different impurity concentrations.

The relationship between the impurity concentration of a gate electrode and the width of a depletion layer

obtained when a voltage is applied to the gate electrode will be described with reference to Fig. 4.

In the MOSFET shown in Fig. 4, a source region 44 and a drain region 43 are formed in the surface portion of a p-well 47. A gate oxide film 42 is formed on the p-well 47 at a portion between these regions 44 and 43. A gate electrode 40 is formed on the gate oxide film 42. A gate voltage Vg is applied to the gate electrode 40, and the p-well 47 is connected to the ground potential. The region of the p-well 47 sandwiched between the drain region 43 and source region 44 forms an inversion layer (channel) 46. In the p-well 47, portions around the source region 44, drain region 43, and inversion layer 46 form a depletion layer 45. When the gate electrode Vg for forming the inversion layer 46 is applied to the gate electrode 40, that part of the gate electrode 40, which is on the side in contact with the gate oxide film 42 forms a depletion layer 41.

The graph of Fig. 5 shows the relationship between the impurity concentration of the gate electrode 40 and the width of the depletion layer 41.

As shown in Fig. 5, the higher the impurity concentration of the gate electrode 40, the smaller a width t_{dep} of the depletion layer 41. The threshold voltage of a MOSFET is determined by a thickness t_{ox} of the

gate oxide film, and in practice by a value $t_{ox} + t_{dep}$ obtained by adding the width t_{dep} of the depletion layer 41 to the thickness t_{ox} of the gate oxide film.

Hence, in the semiconductor device shown in Fig. 3F, since the impurity concentration of the gate electrode 9 is higher than that of the gate electrode 8, the width of the depletion layer of the gate electrode 9 is smaller than that of the depletion layer of the gate electrode 8. Accordingly, the effective electric field acting on the gate oxide film 5 is smaller on the gate electrode 8 than on the gate electrode 9. As a result, although the two MOSFETs having the gate electrodes 8 and 9 have the gate oxide films 5 of the same thickness, the thickness of the gate oxide film 5 of the MOSFET having the gate electrode 8 is electrically thicker, so the obtained gate tunnel current decreases. If the channel concentration stays the same, the threshold voltage of the MOSFET having the gate electrode 8 is higher than that of the MOSFET having the gate electrode 9.

Therefore, in the MOSFETs of the semiconductor device according to this embodiment, even if the gate oxide films have the same thickness, the threshold voltages to be set can be changed by changing the concentrations of the impurities to be implanted in the gate electrodes.

With the same gate oxide film thickness, if the width

of the depletion layer of the gate oxide film of the gate electrode 9 can be increased, the effective thickness of the gate oxide film is increased. Then, the electric field acting on the gate oxide film decreases. Even when a high voltage is applied to the gate electrode 9, no problem occurs in the service life of the gate oxide film.

The isolation region 2 is etched only when removing the sacrificial oxide film 3 shown in Fig. 3B by etching. Even if the number of types of threshold voltage to be set increases, the isolation region 2 will not be etched any further.

Although polysilicon is used as the material of the gate electrode in this embodiment, the material of the gate electrode is not limited to polysilicon. The present invention can be similarly applied when other semiconductor materials such as single-crystal silicon, amorphous silicon, germanium, silicon germanium (SiGe), and gallium arsenide (GaAs) are used.

In this embodiment, n-channel MOSFETs are formed on a semiconductor substrate. However, the present invention is not limited to this, but can similarly be applied when p-channel MOSFETs are to be formed on a semiconductor substrate.

As an impurity to be implanted in the gate electrodes when forming n-channel MOSFETs, antimony (Sb) can be used.

As an impurity to be implanted in the gate electrodes when forming p-channel MOSFETs, boron, indium (In), or a like element can be used.

When antimony (Sb) is used as an impurity to be implanted in n-channel MOSFETs, since it has a low activation rate and accordingly good controllability for a low impurity concentration, it is effective to increase the width of the depletion layer of the electrode of the gate polysilicon. When indium (In) is used as an impurity to be implanted in p-channel MOSFETs, since it has a low activation rate and accordingly good controllability for a low impurity concentration, it is effective to increase the width of the depletion layer of the electrode of the gate polysilicon film.

While the present invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation, and that changes may be made to the invention without departing from its scope as defined by the appended claims.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features. The description of the invention with reference to the drawings is by way of example only.

The text of the abstract filed herewith is repeated here as part of the specification.

In a semiconductor device, a plurality of MOSFETs of one conductivity type having gate electrodes formed out of a semiconductor material are formed on one semiconductor substrate. The gate electrodes of these MOSFETs are implanted with an impurity at different concentrations in accordance with the threshold voltages to be set. This semiconductor device is manufactured by a method including the steps of forming an isolation region and a well on the surface of a semiconductor substrate, forming a gate oxide film on the surfaces of the isolation region and the well, growing a semiconductor material that forms gate electrodes on the surfaces of the gate oxide film and the isolation region, forming a film that prohibits ion implantation on that part of a region of the semiconductor material, which forms MOSFETs, in order to set a high threshold voltage therein, implanting a first impurity in the semiconductor material and removing the film that prohibits ion implantation, patterning the semiconductor material and removing the semiconductor material by etching to form first and second gate electrodes, and implanting a second impurity in the first and second gate electrodes and prospective source/drain regions.

CLAIMS:

1. A semiconductor device in which a plurality of MOSFETs of one conductivity type having gate electrodes formed out of a semiconductor material are formed on one semiconductor substrate, wherein said gate electrodes of said plurality of MOSFETs are implanted with at least one impurity at different concentrations in accordance with threshold voltages to be set.

2. A device according to claim 1, wherein said plurality of MOSFETs of one conductivity type having said gate electrodes formed out of said semiconductor material are n-channel MOSFETs.

3. A device according to claim 2, wherein said impurity to be implanted in said gate electrodes comprises at least one of arsenic, phosphorus and antimony.

4. A device according to claim 1, wherein said plurality of MOSFETs of one conductivity type having said gate electrodes formed out of said semiconductor material are p-channel MOSFETs.

5. A device according to claim 4, wherein said impurity to be implanted in said gate electrodes comprises at least one of boron and indium.

6. A device according to any one of the preceding claims, wherein said semiconductor material that forms said gate electrodes comprises silicon.

7. A semiconductor device manufacturing method comprising the steps of:

forming an isolation region and a well on a surface of a semiconductor substrate;

forming a gate oxide film on surfaces of said isolation region and said well;

growing a semiconductor material that forms gate electrodes on a surface of said gate oxide film and said surface of said isolation region;

forming a film that prohibits ion implantation on that part of a region of said semiconductor material, which forms MOSFETs, in order to set a high threshold voltage therein;

implanting a first impurity in said semiconductor material and removing said film that prohibits ion implantation;

patterning said semiconductor material and removing said semiconductor material by etching to form first and second gate electrodes; and,

implanting a second impurity in said first and second gate electrodes and prospective source/drain regions.

8. A method according to claim 7 wherein, when said MOSFETs to be formed are n-channel MOSFETs, each of said first and second impurities comprises at least one of

arsenic, phosphorus, and antimony.

9. A method according to claim 7 wherein, when said MOSFETs to be formed are p-channel MOSFETs, each of said first and second impurities comprises at least one of boron and indium.

10. A method according to any one of claims 7, 8 and 9, wherein said semiconductor material that forms said gate electrodes is silicon.

11. A semiconductor device substantially as herein described with reference to and as shown in the accompanying drawings.

12. A semiconductor device manufacturing method substantially as herein described with reference to and as shown in the accompanying drawings.

The Patent Office

21

INVESTOR IN PEOPLE

Application No: GB 9924488.1 **Examiner:** COLIN STONE
Claims searched: All **Date of search:** 18 January 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K(KGAGX,KCAL)

Int Cl (Ed.7): H01L

Other: ON LINE,W.P.I.,EPODOC,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2001197 A	MOSTEK	
A	US 5495122	FUJI (See transistors 103,105,Fig.1)	
A	US 4651406	HITACHI (See Fig.2)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.